Remarks/Arguments:

Amendments

No amendments have been made.

First Rejection under 35 USC 103(a)

Claims 11, 12, and 16-21 were rejected as unpatentable over Arita, U.S. Patent 5,624,864 ("Arita") and Shanker, U.S. Patent 4,782,380 ("Shanker"). This rejection is respectfully traversed.

Arita discloses a semiconductor device having a capacitor and a manufacturing method thereof. (See Arita, Title.) The Office admits that Arita does not show heat-treating the TiN layer before depositing the upper aluminum layer after the heat treatment and depositing directly the aluminum layer on the TiN layer using sputtering and heating the circuit board in a temperature range of 100 to 400°C. Office action of 7/15/04, page 3, lines 1-4.

The Office asserts that Shanker teaches (*e.g.*, Figure 1 and column 4 line 38 to column 5 line 23) to heat-treat (*i.e.* anneal) the TiN layer before directly depositing the aluminum upper layer using sputtering and heating the circuit board in a temperature range of 100 to 400°C to improve step coverage (column 2 lines 48 to 53). *Id.*, lines 4-22. This assertion is respectfully traversed.

Shanker does not disclose "depositing an upper metal layer directly on said TiN layer" as recited by step f2c) of independent claim 16, the only independent claim remaining in the application. Shanker discloses formation of an additional layer before the aluminum layer is deposited.

> After formation of the first or lower barrier layer, the vacuum is released or broken to expose the structure to oxygen. This exposure results in the formation of a thin oxide film **44** of about 20-50 Å over the barrier layer which will form a chemical barrier without adversely affecting the electrical contact resistance between the barrier layer and

> a conductive metal layer, such as an aluminum layer, which will subsequently be placed thereon. The exposure of the upper surface of the barrier layer to oxygen at this point in the process is also believed to impregnate or stuff the barrier layer with oxygen between the grain boundaries therein to further inhibit migration through the barrier layer of either the silicon from beneah (sic) or aluminum from above.
>
> Shanker, column 4, lines 24-37 (emphasis added).

In Shanker, an oxide layer is formed on top of the TiN barrier layer. The aluminum layer is deposited on the oxide layer, not directly on the TiN layer. As shown in Figure 1, oxide layer **44** is between barrier layer **40** and conductive metal layer **50**.

As described above, the oxide layer of Shanker inhibits migration through the TiN layer of either silicon from the doped silicon layer or from the upper aluminum layer without adversely affecting the electrical contact resistance between the barrier layer and aluminum layer, and is therefore an essential part of Shanker's invention. Thus, neither Arita, Shanker, nor the combination thereof provide any motivation for the person of ordinary skill in the art to omit the oxide layer and deposit the aluminum layer directly on the TiN layer.

Further, the purpose of the heat treatment is not, as asserted by the Office, to improve step coverage. As stated by Shanker:

> The purpose of the anneal is to improve the electrical contact resistance of the barrier to the doped silicon regions by intimate mixing at the silicon-barrier interface and also formation of a primitive silicide ($TiSi_x$, where x is greater than (1). The anneal also improves the barrier performance by forming a nitride-rich skin such as TiWN or TiN_x (where x is greater than 1) at the surface.
>
> Shanker, column 4, lines 43-51.

As described in applicants' specification, applicants carry out a heat-treatment step to create extensional tensile stress so that the ferroelectric capacitor characteristics are not deteriorated. Specification, page 2, line 16, to page 3, line 6; and page 8, lines 16-24. Neither Arita nor Shanker recognizes that compressional direction stress can cause the characteristics of the device to deteriorate.

The Office has not made a *prima facie* case. The combination of Patel and Shanker in the manner indicated by the Office does not produce applicants' invention. Neither Arita, Shanker, nor the combination thereof discloses or suggests depositing the aluminum layer directly on the TiN layer. Therefore, the rejection of claims 11, 12, and 16-21 as unpatentable over Arita and Shanker should be withdrawn.

Second Rejection under 35 USC 103(a)

Claims 5, 11, 12, and 16-21 were rejected as unpatentable over Patel, U.S. Patent 5,374,578 ("Patel") and Shanker. This rejection is respectfully traversed.

Patel shows a method for forming a ferroelectric capacitor for use in an integrated circuit. (See Patel, Abstract.) The Office admits that Patel does not show heat-treating the TiN layer before depositing the upper Al layer using sputtering and heating the circuit board in a temperature range of 100 to 400°C. Office action of 7/15/04, page 4, lines 1-3.

As discussed above, contrary to the Office assertion, Shanker does not disclose depositing an upper metal layer directly on the TiN layer. Shanker deposits the aluminum layer on an oxide layer, which is an essential part of his invention. Thus, neither Patel, Shanker, nor the combination thereof provides any motivation for the person of ordinary skill in the art to deposit the aluminum layer directly on the TiN layer.

The Office has not made a *prima facie* case. The combination of Patel and Shanker in the manner indicated by the Office does not produce applicants' invention. Neither Patel, Shanker, nor the combination thereof discloses or suggests depositing an upper metal layer directly on the TiN layer. Therefore, the rejection of

claims 5, 11, 12, and 16-21 as unpatentable over Patel in view of Shanker should be withdrawn.

Third Rejection under 35 USC 103(a)

Claim 14 was rejected as unpatentable over Arita, Shanker, and Wolf, Silicon Processing for the VLSI Era, Vol. 1, p.367 (1986) ("Wolf"). This rejection is respectfully traversed.

As discussed above, neither Arita, Shanker, nor the combination thereof discloses depositing an upper metal layer directly on the TiN layer. This deficiency is not overcome by Wolf, which was cited for the disclosure of depositing a SiN using PECVD at an RF power of 300 W or less.

The Office has not made a *prima facie* case. The combination of Arita, Shanker, and Wolf in the manner indicated by the Office does not produce applicants' invention. Neither Arita, Shanker, Wolf, nor the combination thereof discloses or suggests depositing an upper metal layer directly on the TiN layer. Therefore, the rejection of claim 14 as unpatentable over Arita, Shanker, and Wolf should be withdrawn.

Fourth Rejection under 35 USC 103(a)

Claim 14 was rejected as unpatentable over Patel, Shanker, and Wolf. This rejection is respectfully traversed.

As discussed above, neither Patel, Shanker, nor the combination thereof disclose or suggest depositing an upper metal layer directly on the TiN layer. This deficiency is not overcome by Wolf, which was cited for the disclosure of depositing a SiN using PECVD at an RF power of 300 W or less.

The Office has not made the *prima facie* case. Combination of Patel, Shanker, and Wolf in the manner indicated by the Office does not produce applicants' invention. Neither Patel, Shanker, Wolf, nor the combination thereof discloses or suggests depositing an upper metal layer directly on the TiN layer. Therefore, the

rejection of claim 14 as unpatentable over Patel, Shanker, and Wolf should be withdrawn.

Conclusion

It is respectfully submitted that the claims are in condition for immediate allowance and a notice to this effect is earnestly solicited. The Examiner is invited to phone applicants' attorney if it is believed that a telephonic or personal interview would expedite prosecution of the application.

Respectfully submitted,

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